REMARKS

Claims 1-4, 6-14, and 16-22 were pending in this application.

Claims 1-4, 6-14, and 16-22 have been rejected.

No claims have been amended.

Claims 1-4, 6-14, and 16-22 remain pending in this application.

Reconsideration and full allowance of Claims 1-4, 6-14, and 16-22 are respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 1-4, 6-10, and 21 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,805,852 to Nakanishi ("*Nakanishi*") in view of U.S. Patent No. 6,167,501 to Barry et al. ("*Barry*"). The Office Action rejects Claims 11-14, 16-20, and 22 under 35 U.S.C. § 103(a) as being unpatentable over *Nakanishi* and *Barry* in view of U.S. Patent No. 4,591,973 to Ferris, III et al. ("*Ferris*"). These rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce

evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (*MPEP § 2142*).

Claims 1 and 11 recite a "plurality of bypass tristate line drivers" having "output channels" coupled to a "common read data channel." Claims 1 and 11 also recite a "multiplexer" having a "first input channel coupled to [the] common read data channel" and an "output channel coupled to a first operand channel of a first execution unit."

Nakanishi recites various tristate buffers T1-T72 coupled to various buses 1-1 through

4-2. (*Figure 3*). Each of the buses 1-1 through 4-2 provides an input to one of multiple latch circuits L1-L8. (*Figure 3*). The latch circuits L1-L8 provide input operands to arithmetic logic units (ALUs) a1-a4. (*Figure 3*).

Nakanishi does recite the use of multiple tristate elements (buffers T1-T72), and those tristate elements are coupled to common lines (buses 1-1 through 4-2). However, *Nakanishi* lacks any mention of using a "multiplexer" having a "first input channel coupled to [a] common read data channel" and an "output channel coupled to a first operand channel of a first execution unit." For example, *Nakanishi* lacks any mention of a multiplexer coupling one of the buses 1-1 through 4-2 to any of the latches L1-L8 or to any of the ALUs a1-a4.

Moreover, a person skilled in the art has absolutely no motivation to modify *Nakanishi* to include a multiplexer between one of the buses 1-1 through 4-2 and one of the ALUs a1-a4. While *Barry* may illustrate the use of a multiplexer 20, the multiplexer 20 of *Barry* receives multiple input signals and outputs a single output signal. (*Figure 1D*). That is the whole purpose of a multiplexer – receive multiple inputs and select one of the inputs for output. No such functionality is needed in *Nakanishi*.

The tristate buffers T1-T72 of *Nakanishi* function so that data from only one of multiple sources is provided on each of the buses 1-1 through 4-2. The data from each bus is then provided to a single one of the latches L1-L8 and then to a single one of the ALUs a1-a4. As a specific example, tristate buffers T1, T9, T17, T25, T33, T41, T49, T57, and T65 ensure that only one data source is providing data to bus 1-1. Bus 1-1 provides the data to a single destination, which is the left input of ALU a1 through latch L1. The left input of ALU a1

receives input only from one source, which is bus 1-1 through latch L1.

Because of this, there is absolutely no need in *Nakanishi* for a multiplexer coupled between bus 1-1 and the left input of ALU a1. Any multiplexer placed between bus 1-1 and the left input of ALU a1 would receive only one input signal (the signal from bus 1-1). As stated above, the whole purpose of a multiplexer is to receive multiple inputs and select one of the inputs for output. If only one input signal is received, there is no need for a multiplexer.

The tristate buffers T1-T72 of *Nakanishi* allow data from any data source to be provided to any input of the ALUs a1-a4. In other words, proper configuration of the tristate buffers T1-T72 allows data from any source to be provided to an appropriate input of an ALU. As a result, there is no need in *Nakanishi* to use any multiplexers between the buses 1-1 through 4-2 and the ALUs a1-a4. *Nakanishi* already operates to provide a single data signal to each input of the ALUs a1-a4.

The mere fact that two references can be combined is not adequate to establish that a claimed invention is obvious. (*MPEP § 2143.01*). Rather, the Patent Office must establish that the prior art suggests the "desirability" of the combination. (*MPEP § 2143.01*). Here, the Patent Office has simply asserted that the multiplexer of *Barry* (which receives four input signals and produces one output signal) could be used in the system of *Nakanishi*. However, there is no need in *Nakanishi* for the multiplexer of *Barry*. The multiplexer of *Barry* would therefore serve no useful purpose in *Nakanishi* and would simply increase the size, complexity, and cost of the system of *Nakanishi* without providing any benefits. As a result, the Office Action has not established that a person skilled in the art would modify *Nakanishi* to include the multiplexer of

Barry.

For these reasons, the Office Action has not established a *prima facie* case of obviousness against Claims 1 and 11 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejection and full allowance of Claims 1-4, 6-14, and 16-22.

II. CONCLUSION

The Applicant respectfully asserts that all pending claims in this application are in condition for allowance and respectfully requests full allowance of the claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

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